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06EC56

Fifth Semester B.E. Degree Examination, June 2012
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the nMOS fabrication process, with neat diagram. **(10 Marks)**

b. Explain the influence of β_n/β_p on the DC transfer characteristics of inverter. **(05 Marks)**

c. Discuss the difference in the thermal sequence between nMOS and CMOS processes. **(05 Marks)**

2 a. Draw the circuit schematic and stick diagram for CMOS 2 input NOR gate. **(07 Marks)**

b. With neat sketches, explain λ based design rules for pMOS, nMOS and nMOS depletion mode transistor. **(06 Marks)**

c. List the colour, stick encoding, mask layout encoding, layers for a simple metal nMOS process. **(07 Marks)**

3 a. Explain the operation of CMOS dynamic logic. Discuss the merits and demerits. **(06 Marks)**

b. Realize $Z = \overline{A(B+C) + DE}$ for a clocked CMOS logic. **(06 Marks)**

c. What are the properties of nMOS and pMOS switches? How is transmission gate useful? **(08 Marks)**

4 a. What are the scaling factors of
   i) Parasitic capacitance C_X
   ii) Power dissipation per unit area P_a. **(04 Marks)**

b. Calculate the ON resistance for nMOS inverter with R_{sn} = 10 KΩ, Z_{PU} = 8 and Z_{pd} = 1. **(04 Marks)**

c. What are the possible effects of propagation delay in cascaded pass transistor chain and long polysilicon wires? **(12 Marks)**

PART – B

5 a. Explain how to implement the switch logic of four way multiplexer, using transmission gate. **(10 Marks)**

b. Explain the dynamic 4-bit shift register, using nMOs logic. **(10 Marks)**

6 a. Discuss the problems associated in VLSI design. **(04 Marks)**

b. Explain the design steps for a 4-bit adder. **(06 Marks)**

c. Explain 4-bit Braun multiplier, with net diagram. **(10 Marks)**

7 a. Explain the working of one transistor dynamic memory cell, with schematic and stick diagram. **(06 Marks)**

b. Explain nMOS pseudo static memory cell, with stick diagram. **(08 Marks)**

c. Explain the concept of system partitioning in VLSI chip testing. **(06 Marks)**

8 Write short notes on :

a. BICMOS logic

b. CMOS inverter noise margin

c. Built in self test (BIST)

d. Input/output pads. **(20 Marks)**

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